IN THE CLAIMS

Please amend the claims as follows:

Claims 1-20 (Canceled).

Claim 21 (Currently Amended): A semiconductor device comprising:

a semiconductor substrate;

a first main electrode provided on a first main surface of [[a]] said semiconductor substrate; [[and]]

a second main electrode provided on a second main surface of said semiconductor substrate, wherein a main current flows in a thickness direction of said semiconductor substrate[[,]];

a trench that extends from the first main surface of said semiconductor substrate towards the second main surface;

a gate insulating film covering an inner surface of said trench; and

a gate electrode buried in said trench and surrounded by said gate insulating film,

wherein said semiconductor substrate has at least one recess formed in said second main surface and therefore said semiconductor substrate at least has a first region having a first thickness and a second region having a second thickness that is thinner than said first thickness,

said second region corresponds to a region where said at least one recess is formed,

said second main electrode is provided in said at least one recess, and

said second thickness is set at such a thickness as to keep a breakdown voltage of said semiconductor device.

Claim 22 (Previously Presented): The semiconductor device according to claim 21, wherein said second main electrode is formed of a material that makes ohmic contact or Schottky contact with said semiconductor substrate.

Claim 23 (Previously Presented): The semiconductor device according to claim 21, further comprising a semiconductor region provided in a surface of said semiconductor substrate in a portion corresponding to a bottom of said at least one recess, said semiconductor region having a higher impurity concentration than said semiconductor substrate.

Claim 24 (Previously Presented): The semiconductor device according to claim 23, wherein said semiconductor region has a conductivity type opposite to that of said semiconductor substrate.

Claim 25 (Previously Presented): The semiconductor device according to claim 23, wherein said semiconductor region has a same conductivity type as said semiconductor substrate.

Claim 26 (Previously Presented): The semiconductor device according to claim 21, wherein said recess is located substantially in a center of said semiconductor device.

Claim 27 (Previously Presented): The semiconductor device according to claim 21, further comprising an insulating film provided in a surface of said semiconductor substrate in a portion corresponding to a side of said at least one recess.

Claim 28 (Previously Presented): The semiconductor device according to claim 21, further comprising a field contact ring provided in said first main surface of said semiconductor substrate, for alleviating an electric field in a peripheral portion of said semiconductor device,

wherein said second region is provided in an area surrounded by said field contact ring.

Claim 29 (Previously Presented): The semiconductor device according to claim 28, wherein said field contact ring is provided in said first main surface of said semiconductor substrate in a portion corresponding to said first region.

Claim 30 (Previously Presented): The semiconductor device according to claim 21, wherein a side of said at least one recess is inclined at an angle exceeding 90° with respect to said second main surface.

Claim 31 (Withdrawn): The semiconductor device according to claim 21,

wherein said semiconductor substrate has a first conductivity type,

and wherein said semiconductor device further comprises:

a first semiconductor region having a second conductivity type and provided in the entirety of said first main surface of said semiconductor substrate;

a trench formed to extend from said first main surface and pass through said first semiconductor region;

a gate insulating film covering an inner surface of said trench;

a gate electrode buried in said trench and surrounded by said gate insulating film;

a second semiconductor region having said first conductivity type and selectively provided in a surface of said first semiconductor region, a portion of said second semiconductor region being in contact with said gate insulating film;

a third semiconductor region having said second conductivity type and provided in a surface of said semiconductor substrate in a portion corresponding to a bottom of said at least one recess;

a fourth semiconductor region having the first conductivity type and provided in a surface of said first region on said second main surface side; and

a third main electrode in contact with said fourth semiconductor region,

and wherein said first main electrode is in contact with said second semiconductor region, and

said second main electrode is electrically connected to said third semiconductor region.

Claim 32 (Withdrawn): The semiconductor device according to claim 31, wherein said at least one recess is filled with a conductor layer, said third semiconductor region is in contact with said conductor layer, and said second main electrode is provided on a surface of said conductor layer.

Claim 33 (Withdrawn): The semiconductor device according to claim 32, wherein said second main electrode and said third main electrode are formed as a common main electrode extending over both of a surface of said fourth semiconductor region and the surface of said conductor layer.

Claim 34 (Withdrawn): The semiconductor device according to claim 31, further comprising a lifetime control region where carrier lifetime is shortened, said lifetime control region being provided in said first region and closer to said second main surface than said third semiconductor region.

Claim 35 (Withdrawn): The semiconductor device according to claim 31, further comprising a lifetime control region where carrier lifetime is shortened, said lifetime control region being provided in said first region and closer to said first main surface than said third semiconductor region.

Claim 36 (Withdrawn): The semiconductor device according to claim 31, further comprising an insulating film provided on the surface of said semiconductor substrate in a portion corresponding to a side of said recess.

Claim 37 (Withdrawn): The semiconductor device according to claim 31, wherein said recess has such a depth that a distance between a bottom of said third semiconductor region and a bottom of said trench is 100 to 200 μm.

Claim 38 (Withdrawn): The semiconductor device according to claim 31, wherein said recess has a width in the range of 0.2 to 100 μm.

Claim 39 (Previously Presented): The semiconductor device according to claim 21, wherein said first thickness is set in the range of 500 to 650 μm and said second thickness is set at around 60 μm.

Claim 40 (Currently Amended): A semiconductor device comprising:

a semiconductor substrate;

a first main electrode provided on a first main surface of [[a]] said semiconductor substrate; [[and]]

a second main electrode provided on a second main surface of said semiconductor substrate, wherein a main current flows in a thickness direction of said semiconductor substrate[[,]];

a trench that extends from the first main surface of said semiconductor substrate towards the second main surface;

a gate insulating film covering an inner surface of said trench; and

a gate electrode buried in said trench and surrounded by said gate insulating film,

wherein said semiconductor substrate has at least one recess formed in said second main surface and therefore said semiconductor substrate at least has a first region having a first thickness and a second region having a second thickness that is thinner than said first thickness,

and wherein said second thickness is set at such a thickness as to keep a breakdown voltage of said semiconductor device,

said second region corresponds to a region where said at least one recess is formed,

said at least one recess is filled with a conductor layer, and

said second main electrode is provided on a surface of said conductor layer.